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EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/764,476	ARMEZZANI ET AL.
	Examiner	Art Unit
	John B. Vigushin	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continuing Application

1. The present Application is a continuation of parent US Appln. Ser. No. 09/282,842, filed on March 31, 1999, now US Patent No. 6,198,634 B1. The Examiner has reviewed all the prior art cited or relied upon in the above-mentioned parent Application during the examination of the instant Application, as required by the MPEP § 2001.06(b). The Examiner acknowledges the cancellation of Claims 1-25 and the addition of new Claims 26-45 by the Preliminary Amendment filed with the instant Application as Paper No. 3 on Application filing date January 17, 2001. A first action on the merits of Claims 26-45 follows below.

Specification

2. The disclosure is objected to because of the following informalities:

In the Specification:

p.6, line 18: change "benzatriazole" to --benzotriazole--; and change "Benzatrizaole" to --Benzotriazole--.

Appropriate correction is required.

Claim Objections

3. Claims 26, 32, 38, 44 and 45 are objected to because of the following informalities:

In Claim 26, line 21: change "benzatriazole" to --benzotriazole--.

In Claim 32, line 2: delete "flexible".

In Claim 38, line 19: change "benzatriazole" to --benzotriazole--.

In Claim 44, line 19: change "benzatriazole" to --benzotriazole--.

In Claim 45, line 19: change "benzatriazole" to --benzotriazole--.

In Claim 45, line 16: add comma --,-- after "substrate".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 26-45 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

On p.6, lines 13-15 of the Spec., the Applicant discloses that conductive metallic layers lining the substrates are "comprised of a metallic material such as copper, nickel, gold chromium, solder, alloys of solder or combinations of these metals." The Applicant further teaches, in lines17-18 of p.6, that "[w]hen the conductive layers...are comprised of copper, the protective layer is usually a layer of benzatriazole [sic], chlorite, or immersion tin" and goes on to explain the applications of these materials to copper in lines 18-23 of p.6. It is clear that benzotriazole, chlorite and immersion tin are

applicable to copper and to alloys that are predominantly composed of copper. However, these above-mentioned protective layers are evidently not applicable to embodiments of the invention wherein the aperture metallizations are not copper; e.g., nickel, gold, chromium or solder, as disclosed. No disclosure has been made of any contemplated protective layer for those non-copper metals.

Claim 26 recites in lines 12-13 that the conductive metallic layer of the substrate apertures is "selected from the group consisting of copper, nickel, gold, chromium solder and alloys thereof." In lines 18-21, Claim 26 recites that said conductive metallic layer includes "a protective layer thereon, said protective layer selected from the group consisting of benzatriazole [sic], chlorite, and immersion tin." However, these protective layers are enabled **only for the case, as claimed, where the aperture metallic layer is comprised of copper** and evidently not enabled for the case, as claimed, when the aperture metallic layer is comprised of nickel, gold, chromium or solder. Therefore, the claim is non-enabling as a whole since the protective layers benzotriazole, chlorite and immersion tin are supported in the disclosure as only utilized in the case of copper apertures and evidently not for use on the other claimed non-copper aperture metallization limitations. The above-discussed defect of Claim 26 also appears in Claims 38, 44 and 45: See lines 7-10 and 16-19 in Claim 38; lines 7-10 and 16-20 in Claim 44; and lines 7-10 and 16-20 in Claim 45.

6. Claims 27-37 depend from rejected Claim 26 and Claims 39-43 depend from rejected Claim 38 and therefore inherit the above-mentioned defects of Claims 26 and 38, respectively.

Rejections Based On Prior Art

7. The following references were relied upon for the rejections hereinbelow:

Wang et al. (US 6,026,564) Casson et al. (US 5,727,310)

Bindra et al. (US 5,229,550) Crepeau (US 4,249,302)

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 38-41 and 43-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Bindra et al.

As to Claim 38, Bindra et al. discloses: a first circuitized substrate (Fig. 4A) having at least one conductive aperture 8 therein having an external (bottom) surface (Fig. 4A); a second circuitized substrate 11 having at least one conductive aperture 8 therein having an external (upper) surface (Fig. 4B); the first and second substrates aligned such that the conductive apertures of each are substantially aligned (Fig. 4B); the conductive apertures ("wells") of the first and second substrates include a conductive metallic (copper) layer thereon ("copper plated 'wells'"; col.8: 14-15); at least one solder member 2 (Figs. 4A,B; col.5: 14-16: AuSn or SnPb; col.5: 62-66; col.8: 14-17) including a first contact portion (i.e., the bottom portion) extending from said external

(bottom) surface of conductive aperture 8 (Figs. 4A,B), and a second contact portion (i.e., the remaining portion in and beyond conductive aperture 8) substantially within both of the aligned conductive apertures 8 of the first and second circuitized substrates to secure the substrates together (Fig. 4B; col.5: 62-66; col.8: 14-28); the second contact portion of the solder member 2 extends *inherently by capillary action* at least to the external (upper) surface of the conductive aperture metallization of the second conductive substrate 11 (not shown in Figs. 4A,B but taught in col.5: 62-66); the copper material of the conductive apertures 8 of the first and second circuitized substrates including a protective layer of benzotriazole thereon (col.6: 45-55: see table; col.7: 56-58 and 66-68; col.8: 1-3).

As to Claim 39, Bindra et al. further discloses that, *inherently by capillary action*, the second contact portion of solder member 2 is substantially in the form of a dome (similar to the solder dome on either aperture surface of the first circuitized substrate of Fig. 4A) on the external (upper) metallization surface of conductive aperture 8 of second circuitized substrate 11 (dome on substrate 11 not shown, but inherently taught in col.5: 62-66).

As to Claim 40, Bindra et al. further discloses that the second contact portion of solder member 2 is at least one of an array of solder members *inherently* on the *external (upper) surface* (see rejection of base Claim 38, above) of conductive apertures 8 of second circuitized substrate 11 (array of apertures 8 on substrate 11 shown in Fig. 4B).

As to Claim 41, Bindra et al. further discloses that at least one IC chip is attached to the assembled circuitized substrates of Fig. 4B but does not show the chips; the chips inherently are attached to the array of solder members 2 because the solder members 2 form the lands of the assembly that are sufficiently (i.e., closely) spaced for the desired high density chip connections (col.1: 58-62; col.3: 53-55; col.4: 64-col.5: 4).

As to Claim 43, Bindra et al. further discloses that the electronic package of Fig. 4B is a multichip module including at least two chips (col.4: 64-col.5: 4).

As to Claim 44, Bindra et al. discloses: a first circuitized substrate (Fig. 4A) having at least one conductive aperture 8 therein having an external (bottom) surface (Fig. 4A); a second circuitized substrate 11 having at least one conductive aperture 8 therein having an external (upper) surface (Fig. 4B); the first and second substrates aligned such that the conductive apertures of each are substantially aligned (Fig. 4B); the conductive apertures ("wells") of the first and second substrates include a conductive metallic (copper) layer thereon ("copper plated 'wells'"; col.8: 14-15); at least one solder member 2 (Figs. 4A,B; col.5: 14-16: AuSn or SnPb; col.5: 62-66; col.8: 14-17) including a first contact portion (i.e., the bottom portion) extending from said external (bottom) surface of conductive aperture 8 (Figs. 4A,B), and a second contact portion (i.e., the remaining portion in and beyond conductive aperture 8) substantially within both of the aligned conductive apertures 8 of the first and second circuitized substrates to secure the substrates together (Fig. 4B; col.5: 62-66; col.8: 14-28); the second contact portion of the solder member 2 is one of an array of solder members 2 that extends *inherently by capillary action* at least to the external (upper) surface of the

conductive aperture metallization of the second conductive substrate 11 (not shown in Figs. 4A,B but taught in col.5: 62-66); the copper material of the conductive apertures 8 of the first and second circuitized substrates including a protective layer of benzotriazole thereon (col.6: 45-55: see table; col.7: 56-58 and 66-68; col.8: 1-3); at least one chip, not shown in Fig. 4B, wherein the chips *inherently* are attached to the array of solder members 2 because the solder members 2 form the lands of the assembly that are sufficiently (i.e., closely) spaced for high density chip connections (col.1: 58-62; col.3: 53-55; col.4: 64-col.5: 4).

As to Claim 45, Bindra et al. discloses: a first circuitized substrate (Fig. 4A) having at least one conductive aperture 8 therein having an external (bottom) surface (Fig. 4A); a second circuitized substrate 11 having at least one conductive aperture 8 therein having an external (upper) surface (Fig. 4B); the first and second substrates aligned such that the conductive apertures of each are substantially aligned (Fig. 4B); the conductive apertures ("wells") of the first and second substrates include a conductive metallic (copper) layer thereon ("copper plated 'wells'"; col.8: 14-15); at least one solder member 2 (Figs. 4A,B; col.5: 14-16: AuSn or SnPb; col.5: 62-66; col.8: 14-17) including a first contact portion (i.e., the bottom portion) extending from said external (bottom) surface of conductive aperture 8 (Figs. 4A,B), and a second contact portion (i.e., the remaining portion in and beyond conductive aperture 8) substantially within both of the aligned conductive apertures 8 of the first and second circuitized substrates to secure the substrates together (Fig. 4B; col.5: 62-66; col.8: 14-28); the second contact portion of the solder member 2 is one of an array of solder members 2 that

extends *inherently by capillary action* at least to the external (upper) surface of the conductive aperture metallization of the second conductive substrate 11 (not shown in Figs. 4A,B but taught in col.5: 62-66); the copper material of the conductive apertures 8 of the first and second circuitized substrates including a protective layer of benzotriazole thereon (col.6: 45-55: see table; col.7: 56-58 and 66-68; col.8: 1-3); at least two chips, not shown in Fig. 4B, wherein the chips *inherently* are attached to the array of solder members 2 because the solder members 2 form the lands of the assembly that are sufficiently (i.e., closely) spaced for high density chip connections (col.1: 58-62; col.3: 53-55; col.4: 64-col.5: 4).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 26-35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bindra et al. in view of Crepeau and Casson et al.

As to Claim 26:

I. Bindra et al. discloses: a first circuitized substrate (Fig. 4A) having at least one conductive aperture 8 therein having an external (bottom) surface (Fig. 4A); a second circuitized substrate 11 having at least one conductive aperture 8 therein having an external (upper) surface (Fig. 4B); the first and second substrates aligned such that

the conductive apertures of each are substantially aligned (Fig. 4B); the conductive apertures ("wells") of the first and second substrates include a conductive metallic (copper) layer thereon ("copper plated 'wells'"; col.8: 14-15); the first and second circuitized substrates are comprised of polytetrafluoroethylene (PTFE) (col.6: 11-13; col.8: 35-38); at least one solder member 2 (Figs. 4A,B; col.5: 14-16: AuSn or SnPb; col.5: 62-66; col.8: 14-17) including a first contact portion (i.e., the bottom portion) extending from said external (bottom) surface of conductive aperture 8 (Figs. 4A,B), and a second contact portion (i.e., the remaining portion in and beyond conductive aperture 8) substantially within both of the aligned conductive apertures 8 of the first and second circuitized substrates to secure the substrates together (Fig. 4B; col.5: 62-66; col.8: 14-28); the copper material of the conductive apertures 8 of the first and second circuitized substrates including a protective layer of benzotriazole thereon (col.6: 45-55: see table; col.7: 56-58 and 66-68; col.8: 1-3).

II. Bindra et al. teaches that the first circuitized PTFE substrate of Fig. 4A and the second circuitized PTFE substrate 11 of Fig. 4B have a low dielectric constant (col.2: 13-19) and are suitable for high temperature applications (col.8: 35-38) but does not indicate that they are flexible substrates.

III. Crepeau discloses a stacked assembly of flexible circuitized substrates 14, 16 and 18 that are formed of TEFLON which is a PTFE material also having a low dielectric constant for the purpose of enhancing control over signal line impedances (Figs. 1 and 2; col.5: 20-26).

IV. Casson et al. discloses a stacked assembly of including flexible circuitized substrates formed of PTFE material suitable for high temperature applications, the flexibility of the circuitized substrates reducing the mechanical stress on the substrate during operation (col.14: 39-46; col.16: 1-4 and 8-9; col.17: 24-27).

V. Since Bindra et al., Crepeau and Casson et al. are all in the art of stacked substrate packaging, the benefits of the flexible, low dielectric PTFE material for the stacked substrates as taught by Crepeau and Casson et al. would have been readily recognized in the pertinent art of stacked substrate packaging in Bindra et al.

VI. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the low dielectric PTFE material of Bindra et al. with the flexible PTFE materials of Crepeau and Casson et al. in order to reduce the mechanical stress on the stacked substrate package of Bindra et al. due to mechanical shocks during use in an application of the stacked substrate package, as taught by Casson et al., in addition to the low dielectric constant and high temperature application benefits already recognized by Bindra et al. and applied to the stacked PTFE substrates therein.

As to Claim 27, modified Bindra et al. further discloses that the conductive apertures 8 of the first and second flexible circuitized substrates comprise holes having a cylindrical shape (Fig. 4B).

As to Claims 28 and 29, modified Bindra et al. further discloses that solder member 2 is comprised of a high melt solder having a melting point temperature greater

than about 183°C (liquidus temperature for SnPb eutectic, i.e., 63/37, solder) (col.6: 11-13, col.7: 44, col.8: 14-22 and 35-38).

As to Claim 30, modified Bindra et al. further discloses that the first contact portion (i.e., the bottom portion) of solder member 2 extending from the external (bottom) bottom surface of the conductive aperture of the first flexible substrate (Fig. 4A) includes a cross-sectional configuration that is substantially round, oval or ellipsoidal (Fig. 4A).

As to Claim 31, modified Bindra et al. further discloses that the first (bottom) contact portion of the solder member 2 (Fig. 4A) extending from the external (bottom) surface of the conductive aperture 8 of the first flexible circuitized substrate (Fig. 4A) forms a connection to a printed circuit board 12 (Fig. 4B).

As to Claims 32 and 33, modified Bindra et al. further discloses that the second contact portion of the solder member 2 extends *inherently by capillary action* at least to the external (upper) surface of the conductive aperture metallization of the second flexible circuitized substrate 11 (not shown in Figs. 4A,B but taught in col.5: 62-66) and is *inherently* (also by capillary action) in the shape of a dome on said external (upper) surface similar to the dome-shaped contact portions of solder members 2 on the upper and lower aperture surfaces of the pre-assembly structure of the first flexible circuitized substrate of Fig. 4A.

As to Claim 34, modified Bindra et al. further discloses that the second contact portion of the solder member 2 is one of an array of solder members 2 that extends *inherently by capillary action* at least to the external (upper) surface of the conductive

aperture metallization of the second flexible circuitized substrate 11 (not shown in Figs. 4A,B but taught in col.5: 62-66).

As to Claim 35, modified Bindra et al. further discloses that at least one IC chip, not shown in Fig. 4B, wherein the chips *inherently* are attached to the array of solder members 2 because the solder members 2 form the lands of the assembly that are sufficiently (i.e., closely) spaced for high density chip connections (col.1: 58-62; col.3: 53-55; col.4: 64-col.5: 4).

As to Claim 37, modified Bindra et al. further discloses that the package is a multichip module including at least two chips, not shown in Fig. 4B (col.1: 58-62; col.4: 64-col.5: 4).

12. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bindra et al. in view of Crepeau and Casson et al., as applied to claim 26 above, and further in view of Wang et al.

I. Bindra et al. in view of Crepeau and Casson et al. discloses all the limitations of base Claim 26 and also teaches plural IC chips mounted thereon (Bindra et al.: col.1: 58-62 and col.4: 64-col.5: 4) but does not teach that the package of Fig. 4B is a single chip carrier.

II. Wang et al. teaches an assembly of three stacked substrates that is a single chip carrier (Fig. 4; col.5: 21-25).

III. Since both modified Bindra et al. and Wang et al. disclose an assembly of stacked substrates, the use of the assembly as a carrier of a single IC chip appropriate

for an electronic application, taught by Wang et al., would have been readily recognized in the pertinent art of modified Bindra et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the plural chip mounting in the stacked substrate package of modified Bindra et al. by mounting only a single IC chip on the package, as taught by Wang et al., in order to meet the specifications of an electronic application requiring solely the function of that particular chip on the electronic package of modified Bindra et al.

13. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bindra et al. in view of Wang et al.

I. Bindra et al. discloses all the limitations of base Claim 38 and also teaches plural IC chips mounted thereon (col.1: col.58-62; col.4: 64-col.5: 4) but does not teach that the package of Fig. 4B is a single chip carrier.

II. Wang et al. teaches an assembly of three stacked substrates that is a single chip carrier (Fig. 4; col.5: 21-25).

III. Since both Bindra et al. and Wang et al. disclose an assembly of stacked substrates, the use of the assembly as a carrier of a single IC chip appropriate for an electronic application, taught by Wang et al., would have been readily recognized in the pertinent art of Bindra et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the plural chip mounting in the stacked substrate package of Bindra et al. by mounting only a single IC chip on the package, as taught by

Wang et al., in order to meet the specifications of an electronic application requiring solely the function of that particular chip on the electronic package of Bindra et al.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Anzawa et al. (US 5,617,300) discloses substrates 10 and 11 joined through aligned apertures 2h and 3h by means of solder H which extends from a bottom surface of the aperture 2h of substrate 10 (Fig. 5; col.5: 15-23).

b) Boggs (US 4,935,584) discloses rigid or flex substrates (col.1: 37-40) in stacked arrangement by means of solder members 50 and 60 that fill the apertures (Fig. 4; col.3: 47-50 and 57-61).

c) Anthony (US 4,394,712) discloses silicon-on-sapphire substrates 30 joined by solder members 26 in plated apertures 20 of the substrates 30 (Figs. 5, 7 and 8; col.5: 38-46).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
September 26, 2002